SEMESTER S7

ELECTRONIC DESIGN AUTOMATION

Course Code	PEAET741	CIE Marks	40
Teaching Hours/Week (L:T:P:R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	-	Course Type	Theory

Course Objectives:

1. To understand the algorithm behind electronic design automation based on graph theory
2. To familiarize algorithms used for partitioning and layout compaction in Integrated circuits
3. To equip with placement and routing algorithm used in VLSI industry

SYLLABUS

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Module No.	Syllabus Description	Contact Hours
1	Graph Terminology - Basic graph theory terminology, Data structures for representation of graphs. Graphs Search Algorithms - Breadth First Search, Depth First Search, Topological Sort. Shortest Path Algorithms - Dijkstra's Shortest Path Algorithm and Floyd Warshall Algorithm	9
2	Design Automation - VLSI Design Flow, VLSI Design Styles Partitioning Algorithms - Kernighan-Lin Algorithm, Fiduccia-Mattheyses Algorithm (Basic algorithmic description only) Layout - Layout Layers and Design Rules, Physical Design Optimizations	9
3	Compaction - Applications of Compaction Maximum Distance Constraints. Placement - Wirelength Estimation, Weighted Wirelength, Maximum Cut Size, Wire Density. Placement Algorithm - Quadratic Placement. Floor planning - Slicing Floorplan, Non-Slicing Floorplan Floorplan Representations - Constraint Graph, Sequence Pair	9

4	Global Routing - Terminology and Definitions Maze Routing Algorithm - Lee's Algorithm Detailed Routing - Horizontal and Vertical Constraint Graph Channel Routing Algorithm -Left-Edge algorithm Basic concepts of Static Timing Analysis	**9**

Course Assessment Method

(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

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End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24 Marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 Marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Apply Search Algorithms and Shortest Path Algorithms to find various graph solutions.	**K3**
CO2	Outline VLSI Design Flow and Design Styles and apply partitioning algorithms on graphs representing netlist	**K3**
CO3	Illustrate Design Layout Rules and apply different algorithms for layout compaction	**K3**
CO4	Make use of various algorithms to solve placement, floorplan and routing problems	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

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	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2		3							3
CO2	3	3	2		3							3
CO3	3	3	2		3							3
CO4	3	3	2	2	3							3

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	VLSI Physical Design: From Graph Partitioning to Timing Closure	Jin Hu, Jens Lienig, Igor L. Markov, Andrew B. Kahng	Springer	2011
2	Algorithms for VLSI Design Automation	Gerez,S abih H	John Wiley & Sons	2006
3	Algorithms for VLSI Physical Design Automation	Sherwani, Naveed A	Kluwer Academic Publishers,	1999

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	VLSI Physical Design Automation: Theory and Practice	Sadiq M. Sait and H. Youssef	World Scientific	1999
2	CMOS VLSI Design : A circuits and systems perspective	Neil H. E. Weste and David Money Harris	Pearson	4th Edition, 2015
3	VLSI Design Methodology Development	Thomas Dillinger	Pearson	1st Edition, 2020

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://nptel.ac.in/courses/106105161
2	https://nptel.ac.in/courses/106105161
3	https://nptel.ac.in/courses/106105161
4	https://nptel.ac.in/courses/106105161

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