SEMESTER S4

DIGITAL SYSTEM DESIGN

Course Code	PECPT411	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3-0-0-0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. To develop an in-depth understanding of clocked synchronous and asynchronous sequential networks.
2. To summarize the architecture and applications of programmable logic devices.
3. To compare various modeling techniques using Verilog HDL.
4. To construct combinational and sequential circuits using Verilog HDL

SYLLABUS

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Module No.	Syllabus Description	Contact Hours
1	**Analysis of clocked Synchronous Sequential Networks(CSSN):** Modelling of CSSN – State assignment and reduction, Design of CSSN **Analysis of Asynchronous Sequential Circuits (ASC):**Flow table reduction- Races in ASC,State assignment problem and the transition table- Design of AS	9
2	**Programmable Devices:** Architecture of Programmable Array Logic and PLA, Architecture description of Field Programmable Gate Array and Complex Programmable Logic Devices, Case studies of robotic application using FPGA/CPLD.	9
3	Gajski's 'Y' Chart, Behavioral Modeling, Data flow modeling, Structural modeling **Hardware Description Language:** Structure of Verilog module, Operators, Data Types, Styles of Description. Verilog Data flow	9

	description: Highlights of Data flow description, Structure of Data flow description.	
4	**Verilog Behavioral description:** Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioral Description of Multiplexers (2:1, 4:1, 8:1). **Verilog Structural description:** Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder**.**	**9**

Course Assessment Method

(CIE: 40 marks , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

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End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
2 Questions from each module. Total of 8 Questions, each carrying 3 marks **(8x3 =24 marks)**	Each question carries 9 marks. Two questions will be given from each module, out of which 1 question should be answered. Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Construct clocked synchronous sequential networks.	**K3**
CO2	Model asynchronous sequential circuits.	**K3**
CO3	Develop digital systems on FPGAs and CPLDs, and apply them in robotic applications	**K3**
CO4	Demonstrate the structure, types and data flow of Verilog code for combinational and sequential circuits.	**K2**
CO5	Compare digital systems using behavioural and structural Verilog descriptions.	**K2**

Note: *K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

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CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	2									
CO2	3	2	3									
CO3	3	2	3		3							
CO4	3	2	2		2							
CO5	3	2	3		2							

1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Principles & Design	Donald G Givone	Tata McGraw Hill	1/e, 2003
2	HDL Programming VHDL and Verilog.	Nazeih M Botros,	Dreamtech press	3/e, 2009

3	Introduction to Digital Design Using Digilent FPGA Boards,	Richard E. Haskell, Darrin M. Hanna	LBE Books- LLC Understanding	3/e, 2011

Reference Books

Sl. No	Title of the Book	Name of the Author/s	Name of the Publisher	Edition and Year
1	Introduction to Digital Systems	M. Ercegovac, T. Lang and L.J. Moreno	Wiley	1/e, 2000
2	Digital Design	John F Wakerly	Pearson Education	3/e, 2002
3	Verilog HDL: A Guide to Digital Design and Synthesis	Samir Palnitkar	Pearson Education	2/e, 2003
4	Advanced Digital Design with the Verilog HDL	Michael D Ciletti	Pearson education	2/e, 2017

Video Links (NPTEL, SWAYAM…)

Module No.	Link ID
1	https://youtu.be/X7M3rUxUpOc
2	https://youtu.be/Y8FvvzcocT4
3	https://youtu.be/BoIOLczVulQ
4	https://nptel.ac.in/courses/117106114

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