SEMESTER S5
VLSI DESIGN

Course Code	PEICT526	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

1. This course aims to develop the skill to design various VLSI circuits

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Overview of CMOS device fundamentals . The CMOS inverter: - Voltage Transfer Characteristics, SPICE Description, Static Behavior - Switching Threshold - Noise Margins, Dynamic behavior - Device Capacitances - Propagation Delay - Power Consumption.	9
2	CMOS fabrication Processes: -N-Tub, P-Tub and Twin Tub. MOS Circuit Layout - Stick diagrams, Layout design rules, Transistor layout - PMOS and NMOS, Gate Layout - Inverter, NAND, NOR and XOR, Layout generation using MICROWIND tool (For Assignments/Projects only).	9
3	Combinational logic Circuits: - Static MOS - Complementary MOS - Ratioed logic - Pass Transistor logic - Differential Pass Transistor Logic - Transmission gate logic, Dynamic MOS - Basic Principles - Speed and power Dissipation - Signal Integrity issues.	9
4	Sequential Logic Circuits: -Timing Metrics for sequential circuits, Static Latches and Registers, Dynamic Latches and Registers. Datapath Subsystems: - Adder - Ripple carry Adder - Full adder - Carry chain Adder - Carry-Bypass Adder - Carry Select Adder - Carry Look Ahead Adder, Multiplier - Array Multiplier - Carry Save Multiplier, Shifter - Barrel Shifter - Logarithmic Shifter.	9

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Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

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Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	explain the fundamentals of CMOS devices and analyze the behavior of CMOS inverters	**K2**
CO2	Understand CMOS fabrication processes and develop skills in MOS circuit layout	**K2**
CO3	design and analyse sequential logic circuits, including static and dynamic latches and registers, and understand timing metrics for sequential circuits.	**K3**
CO4	design and analyze various combinational logic circuits using different MOS logic styles	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3											2
CO2	3				3							2
CO3	3											2
CO4	3											2

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Integrated Circuits- A Design Perspective	J.M. Rabaey, A. Chandrakasan and B. Nikolic	PHI.	2nd edition 2002
2	Basic VLSI Design	Douglas A. Pucknell & Kamran Eshraghian	PHI	3rd edition
3	CMOS digital integrated circuits: Analysis and design	Sung-Mo Kang, Yusuf Lablebici	TATA McGraw-Hill	4th edition 2015

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Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	CMOS Logic Circuit Design	John P. Uyemura	Springer India Pvt. Ltd. New Delhi.	1st edtion 2001
2	Analysis &Design of Digital Integrated Circuits	David A. Hodges, Horace G. Jackson, R. Saleh	McGraw Hill.	3rd edition
3	CMOS VLSI Design, a Circuits and Systems Perspective,	Neil H. E. Weste, David Money Harris, Addison-Wesley	Pearson	4th edition 2010
4	VLSI Circuit Layout: theory and design	T.C Hu, Ernest S. Kuh	IEEE Press	1st edition 1985

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://onlinecourses.nptel.ac.in/noc21_ee09/preview
2	https://archive.nptel.ac.in/courses/108/101/108101089/
3	https://archive.nptel.ac.in/courses/117/106/117106086/
4	https://www.youtube.com/watch?v=ibQBb5yEDlQ

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